Application No.: 10/830,107

AMENDMENT TO CLAIMS

1. (Currently amended) An information memory and reproduction device comprising:

a variable gain amplifier for amplifying an input analog signal to a predetermined amplitude level and outputting the amplified analog signal;

a low-pass filter for removing a noise component of the amplified analog signal;

an A/D [[convert]] converter for converting the analog signal output from the low-pass filter into a first digital signal and outputting the first digital signal;

a digital equalizer for performing wave-form equalization to the first digital signal and outputting a second digital signal;

an amplitude information detection circuit for detecting amplitude information from the first digital signal, generating control information from the detected amplitude information and outputting the control information to the variable gain amplifier;

a clock extraction circuit for extracting a synchronous clock signal from the second digital signal and outputting the extracted clock signal to the A/D converter and the digital equalizer; and

a frequency divider for dividing an output from the clock extraction circuit and outputting the divided output,

wherein the clock extraction circuit outputs to the A/D converter and the digital equalizer a sampling clock signal having an n times higher frequency than a frequency which defines a channel clock (where n is 2 or a larger integer than 2), and

wherein the A/D converter performs oversampling by the input sampling clock signal.

2. (Original) The information memory and reproduction device of claim 1, further comprising a data phase comparator for selecting one of **n** different sampling values contained in the second digital signal and outputting a selected sampling value to the clock extraction circuit.

3. (Original) The information memory and reproduction device of claim 1, further comprising a moving average value operational unit for selecting adjacent two of **n** different sampling values contained in the second digital signal, performing an operation to selected two sampling values to obtain a moving average, and outputting a sampling value as an operation result to the clock extraction circuit.

4. (Original) The information memory and reproduction device of claim 1, further comprising a moving average value operational unit for selecting at least two of **n** different sampling values contained in the second digital signal, performing an operation to selected at least two sampling values to obtain a moving average, and outputting a sampling value as an operation result to the clock extraction circuit.

5. (Original) The information memory and reproduction device of claim 1, further comprising a sampling value operational unit for selecting at least two of **n** different sampling values contained in the second digital signal, performing an addition operation, a subtraction operation or an interpolation operation to selected at least two sampling values, and outputting a sampling value as an operation result to the clock extraction circuit.

6. (Original) The information memory and reproduction device of claim 1, further comprising a filter for removing an unnecessary signal component from an output signal from the sampling value operational unit, the filter being provided between the sampling value operational unit and the clock extraction circuit.

7. (Original) The information memory and reproduction device of claim 1, further comprising a downsampling circuit for changing a frequency of the second digital signal back to the frequency which defined a channel rate.

8. (Original) The information memory and reproduction device of claim 1, further comprising an offset control circuit for adjusting a shift from a center axis of an amplitude of the analog signal so that the analog signal is located within a dynamic range of the A/D converter, the offset control circuit being provided in a previous stage of the A/D converter.

9. (Original) The information memory and reproduction device of claim 8, further comprising:

an offset detection circuit for detecting an offset of an input analog signal from the first digital signal and outputting a value for a detected offset to the offset control circuit;

an operational circuit for improving reliability of the second digital signal; and

a binarizer circuit for performing binaization to the second digital signal.

10. (Original) The information memory and reproduction device of claim 1, wherein the clock extraction circuit includes a voltage control oscillator.

11. (Original) The information memory and reproduction device of claim 1, wherein the clock extraction circuit includes a phase synchronous loop circuit.